REMARKS

The Office Action of July 12, 2004 has been received and its contents carefully noted. The allowance of claim 6 has been noted with satisfaction.

The present Amendment corrects inadvertent informalities in the specification that were discovered during review of the application. It also makes improvements of a formal nature in claim 6 (the word "the" has been added at several places).

The present Amendment also cancels objected-to claim 5, and transfers it subject matter (with improvements of a formal nature) to claim 1. However, the limitations of claim 4 (from which claim 5 formerly depended) have not been included in claim 1 in the present Amendment, and claim 4 remains as a dependent claim. It is nevertheless respectfully submitted that the invention defined by claim 1 remains patentable over the Kaminaga et al reference, which neither discloses nor suggests an "N-well control circuit" having the features that are now set forth in claim 1.

Since claims 2-4 depend from claim 1 and recite additional limitations to further define the invention thereof, they are patentable along with claim 1 and need not be further discussed.

Section 1 of the Office Action objects to the term "a fourth NMOS transistor" in claim 5. This has been changed to a "third" NMOS transistor in the amendment to claim 1. Accordingly, the objection should be withdrawn.

The present Amendment adds new claims 7-10 to further protect the invention. Claim 7 is independent and the rest are dependent. The new claims are supported (for example) by Figure 3 of the application's drawings. For the reasons discussed below, it

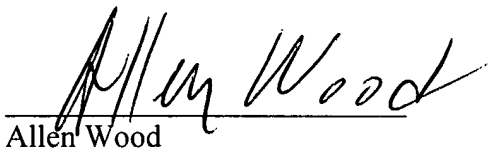
is respectfully submitted that the new claims are patentable over the Kaminaga et al reference.

Claim 7 recites a second NMOS transistor and "a third PMOS transistor having ... a drain coupled to the source of the second NMOS transistor." This is not suggested by Kaminaga et al. Nor would the Kaminaga et al reference have provided an incentive for an ordinarily skilled person to modify the buffer circuit disclosed in the reference so as to achieve a buffer circuit with the third PMOS transistor of claim 7.

Claims 8-10 depend from claim 7 and recite additional limitations to further define the invention, so they are patentable along with claim 7 and need not be further addressed.

For the foregoing reasons, it is respectfully submitted that this application is now in condition for allowance. Reconsideration of the application is therefore respectfully requested.

Respectfully submitted,



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